

Rambus Conference Call: Hynix Trial Update

April 24, 2006

Rambus[®]

Hynix vs. Rambus

- U.S. District Court for the Northern District of CA
- Jury verdict:
 - All 10 Rambus claims found valid and infringed
 - Damages awarded: \$306.9M
 - Covers Hynix memory products sold in the U.S. from June 2000 to the end of 2005
 - SDRAM damages \$30.5M
 - DDR and DDR2 SDRAM damages \$276.4M
- Third phase of trial tentatively set for summer 2006

Infineon: March 31, 1994

TO	FROM	Received stamp/note
Mr. Penzel	HL ST E DER	
HL GP	Responsible W. Meyer	
Mch-B/MN	Mch B	
	Tel. 94-8650	
	Fax. 94-3907	
	e-mail: meyer@vincent.hi.siemens.de	

Your Ref and your message dates: Our Ref: Place and date: Mch B, March 31, 1994

Place and date
Mch B, March 31, 1994

Subject: RAMBUS Seminar, April 14, 1994; Your fax to Dr. v. Zitzewitz dated March 30, 1994

The same thing was tried via Dr. Schumacher: we refused then, too!

It's just a publicity event! Not interesting in terms of development because:

The top
The tec

One day all computers will (have to) be built like this, but hopefully without the royalties going to RAMBUS.

I have already seen the demonstration with Richard C. Crisp (RAMBUS colleague with JEDEC). You really can put video images on the screen. There were a dozen or so of this sort at the CBIT, without RAMBUS.

None of our customers has – as far as I know – included RAMBUS DRAMs in their purchase spectrum. *No demand, no chip.*

Some users (Silicon Graphics, Nintendo, Apple) are currently discussing RAMBUS as a replacement for VRAM.

RAMBUS should first of all secure a sustainable base among our customers. RAMBUS is not a memory, it is a memory system including controller, bus, interface, protocol and memory. **One day all computers will (have to) be built like this, but hopefully without the royalties going to RAMBUS.**

Sincerely,

cc. Dr. v. Zitzewitz

SD 1432796



OUTSIDE COUNSEL ONLY
UNDER PROTECTIVE ORDER
E.D. VA. CA. 00-124
1251805

TRANSLATION

PTX 846A

Rambus®

Hynix: "Kil" Memo – October 17, 1992 (p. 1 of 4)

*(handwritten memo; portions illegible; SIC)
 NEC, Fujitsu Market Research*

Semiconductor Application Technology Department Technical Report		Summary of Technical Evaluation on RAMBUS ARCHITECTURE	
Title		Summary of Technical Evaluation on RAMBUS ARCHITECTURE	
Reporter	Kil, Sung-Bum	Date	1992. 10. 17 [sic., illegible]
Product Group	Area	Evaluator of Technology	
1. Memory	1. Application Tech.	Approved by	Div. Head
2. LOGIC	2. Failure Analysis		Director
3. ASIC	3. Technical Evaluation		General Mgr.
4. MPUMCU	4. Market Analysis		Ho, Kyu-hwan
5. Misc.	5. Misc.		[sig.]

Date 1992. 10. 17 [sic., illegible]

Purpose

To summarize what has been made known regarding Rambus interface and Rambus DRAM, both developed by the US-based venture capital concern known as Rambus [company] in 1990, and to conduct an evaluation vis-à-vis our Company's particular requirements/needs, in the hopes of aiding in the establishment of the [Company's] next generation product and the undertaking thereof.

Rambus Architecture

A new architecture as reported on in March of 1992 and comprised of a Rambus Channel, Rambus Interface and Rambus DRAM, in which a data transmission [speed] of 500 MByte/sec. is possible. Fujitsu, NEC and Toshiba have entered into a license agreement and are developing Rambus DRAM, Rambus Interface Logic, etc. with a 4M Bit followed by a report on related its particular performance [characteristics].

A new architecture as reported on in March of 1992 and comprised of a Rambus Channel, Rambus Interface and Rambus DRAM.

Rambus DRAM

A DRAM specially designed to have a 200 MByte/sec. data transmission speed through its Rambus Channel comprising of a generic DRAM memory cell, a cache-function sense amp, a small voltage swing, and through the elimination of pin-to-pin noise and the skew. Should the Rambus DRAM become a standard, a market is expected to form in full-fledged fashion for high speed applications. Additional applications are expected to be in those areas considered largely unrelated to the overall configuration of the system and therefore easier to apply, such areas as animation and 3-D graphics which require real-time display.

Should the Rambus DRAM become a standard, a market is expected to form in full-fledged fashion for high speed applications.

[Ref. 1]: Given that Synchronous DRAM controller for the same is [relatively] feasible data access rate of 100 MHz there is expected to be a disparity in the target market in comparison to Rambus DRAM.

[Ref. 1]: Given that Synchronous DRAM operates within TTL compatible logic and the development of a controller for the same is [relatively] feasible, a market is expected quickly to form, but with a maximum data access rate of 100 MHz there is expected to be a disparity in the target market in comparison to Rambus DRAM.

[Ref. 2]: EDAM (Enhanced DRAM), developed by the US-based Ramtron company and [mass] produced by Mitsubishi, has a very similar architecture to Rambus' internal operations (DRMA memory cell and cache SRAM sense amp), and has a data transmission speed of 100 MHz. Although Synchronous DRAM is identical in terms of transmission speed, [this is] asynchronous in its operation. Standardization concerning this product also is expected.

Distribute to: Marketing Dept. 1

¹ Slight techno-linguistic ambiguity

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Hynix: "Kil" Memo – October 17, 1992 (p. 2 of 4)

1.0 Purpose

To summarize what has been made known regarding Rambus Interface and Rambus DRAM, both developed by the US-based venture capital concern known as Rambus [company] in 1990, and to conduct an evaluation vis-à-vis our Company's particular requirements/needs, in the hopes of aiding in the establishment of the [Company's] next generation product and the undertaking thereof.

2.0 Rambus Incorporation [sic]

- 2.1 Establishment [sic] Scholar Horowitz (C
- 2.2 Investment: three compar
- 2.3 Chairman: E
- 2.4 President: G
- 2.5 COO/VP: D (Manager)
- 2.6 CTO/VP: A
- 2.7 Address: 246
- 2.8 Employees: 1
- 2.9 Management

1.0 Purpose

To summarize what has been made known regarding Rambus Interface and Rambus DRAM, both developed by the US-based venture capital concern known as Rambus [company] in 1990, and to conduct an evaluation vis-à-vis our Company's particular requirements/needs, in the hopes of aiding in the establishment of the [Company's] next generation product and the undertaking thereof.

3.0 Rambus Architecture

A new architecture as reported on in March of 1992 and comprised of a Rambus Channel, Rambus Interface and Rambus DRAM, in which a data transmission [speed] of 500 MByte/sec. is possible. Fujitsu, NEC and Toshiba have entered into a license agreement and are developing Rambus DRAM, Rambus Interface Logic, etc. with a 4M Bit Rambus DRAM sample expected to come out by the end of 1992, followed by a report on related interface chips by 1993, whereby which it will be made clear as to the particular performance [characteristics] and market.

3.1 Rambus Channel

- 1) Noise reduction and speeding up of signal transition time based on a Logic high-low swing of 0.6 V.
- 2)

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Hynix: "Kil" Memo – October 17, 1992 (p. 3 of 4)

4.0 Status on the Development of Related Products & Industry Interest

4.1 Toshiba

- 1) Planning to introduce 4.5M Bit RDRAM "TC59RD4MRVR" [sic; illegible] around July-Sept. of 1992 (no report made on it to date).
- 2) Planning to introduce an 18M RDRAM sample during Q2 of 1993.
- 3) Currently in development for a Bridge Chip for R400PC RISC for a US PC Manufacturer.
- 4) Market Forecast: of the overall DRAM market during 1995-1997.
 - Existing generic DRAM: 50%
 - Rambus DRAM: 25%
 - Synchronous DRAM: Expected to stake out 25% of the market

★4.2 NEC

- 1) Planning to produce 4M DRAM provided there is demand.
- 2) Planning to introduce an 18M DRAM "uPD488170" [sic.] during Q1 of 1993.
- 3) Planning to introduce a 16M DRAM "uPD488130" [sic.] during Q2 of 1993.
- 4) Planning to introduce a Bridge for R4000 purposes to serve as the main memory cache and perform the function of graphic cache, during Q2 of 1993.

★

4.3 Fujitsu

- 1) Planning to introduce a 4M RDRAM sometime during 1992.
- 2) Planning to introduce an 18M RDRAM sometime during 1993.
- 3) Planning to introduce sometime during 1993 a SPARClike microprocessor incorporating a Rambus interface.
- 4) Planning to introduce sometime during 1993 a Bridge chip for i486DX purposes.

4.4 Rambus, Inc.

- 1) The first application will be in the animation and 3D-graphic market, which requires real-time display. The second RDRAM will be of a 2M x 9-bit configuration having either a 4 or 8 bank [array], and a product operating at 3.3 V also may be possible.
- 2) RDRAM anticipated to comprise 50% of the DRAM market after 1995.

4.5 Intel

- 1) Adoption of the Rambus architecture inevitable after 2-5 years.
(General Manager of Workgroup Computing Division)
- 2) Currently looking into it (Vice President).

4.5 Intel

- 1) Adoption of the Rambus architecture inevitable after 2-5 years.

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Hynix: "Kil" Memo – October 17, 1992 (p. 4 of 4)

Development of ASIC technology for the development of a Transceiver incorporating a generic-purposes Bridge Chip and a plurality of PLL circuits.

5.2 Assembly and Testing

- 1) Development of a 32-pin VSMP (Vertical Surface Mount Package) technology. -- 25.6 mil lead pitch, 950 mil wide, 460 mil height, 47 mil thick.
- 2) Development of the Test Concept; Test Algorithm; Tester; and Interface Board, in order to guarantee operation at 250 MHz.
- 3) Development of a PCB for Rambus DRAM module purposes in order to satisfy Rambus channel requirements.
*US-based company Augit develops a standard Rambus channel board in concert with Rambus, Inc.

6.0 Epilogue

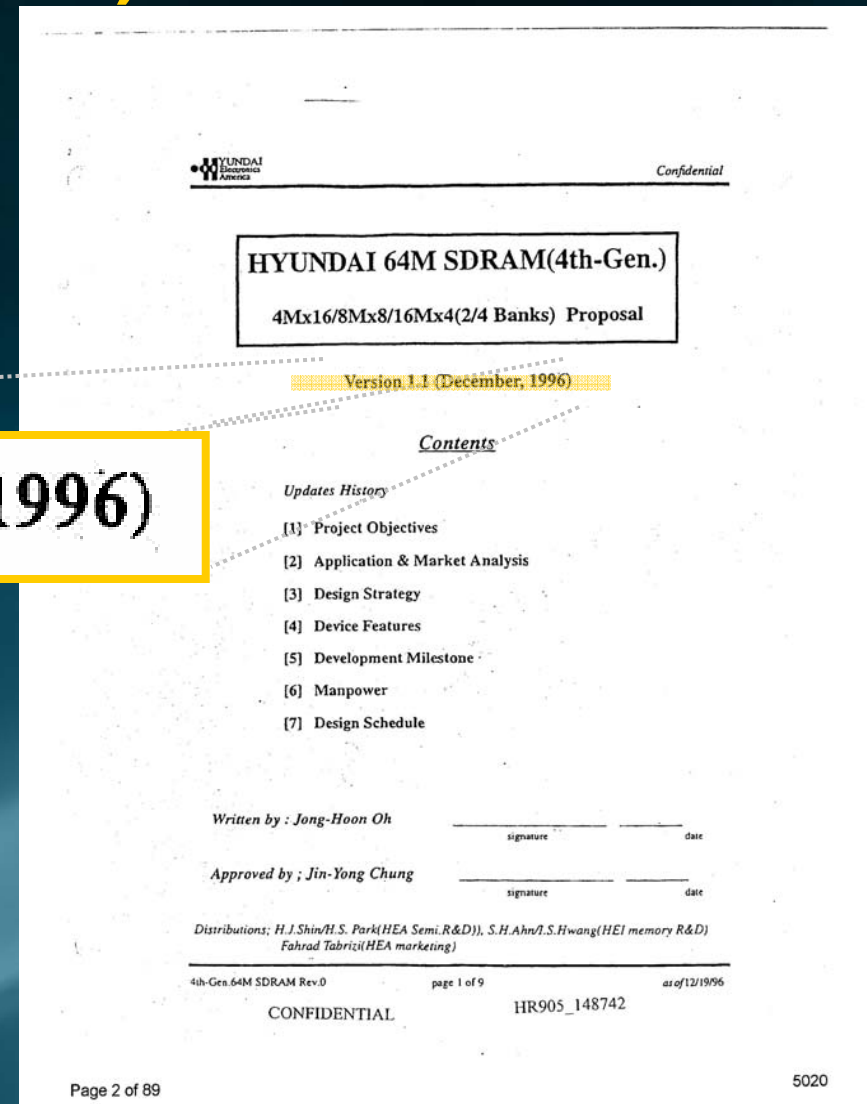
- 6.1 Whereas Microprocessors have been continually undergoing performance improvements based on the adoption of superscalar and super-pipelined architectures, etc., the speeds of memory elements—especially that of the DRAM used as main memory—have not been able to support such advances; the problem has been partially addressed by way adopting an internal primary cache and an external secondary cache within the microprocessor, yet has inevitably been accompanied by the consequent increase in power consumption and rise in production costs.
- 6.2 Moreover, when operating at 50 MHz or higher, the current PCB material and architecture have not been able to accommodate the radical voltage swings and limitations in impedance control, etc., such that the PCB architecture, heretofore viewed in terms of its simple, interconnection function only, now is interpreted as being a transmission conduit, wherein which the new problem of having accordingly to lay out and connect the chips has arisen.
- 6.3 Additionally, although there have been speed improvements up to several hundred MHz's based on the adoption of an ECL interface, the non-compatibility of the logic levels and the ECL's non-saturated operational characteristics have resulted in an excessively high rate of power consumption; generation of a high level of heat, etc., further necessitating the use of costly ceramic package [material]; cooling system[s]; large[r] power supply, etc., ultimately resulting in drastic increases in system cost.
- 6.4 Against such a backdrop, the appearance of Synchronous DRAM and Rambus DRAM has resulted in new hopes on the part of many a system developer.
- 6.5 In the hope of having the many semiconductor companies and systems companies adopt it as a standard, Synchronous DRAM has been making many efforts in JEDEC meetings, such that a standardized Synchronous DRAM sample is expected to come out sometime during 1993.
- 6.6 Synchronous DRAM is operable at [the level of] TTL compatible logic, with the development of a controller for it being quite feasible; yet, with a maximum data access rate of 100 MHz, there is anticipated to be a large disparity within the target market, in comparison to Rambus DRAM.
- 6.7 Further follow functions/featu

6.6 Synchronous DRAM is operable at [the level of] TTL compatible logic, with the development of a controller for it being quite feasible; yet, with a maximum data access rate of 100 MHz, there is anticipated to be a large disparity within the target market, in comparison to Rambus DRAM.

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Hynix 64M SDRAM Specification December 1996 (p. 1 of 2)

Version 1.1 (December, 1996)



Hynix 64M SDRAM Specification December 1996 (p. 2 of 2)

CLK buffer for OE

- DLL circuit^d will be employed to compensate clock-to-output delay for better tAC.
- Double clock edges are used at DDR mode. The duty ratio of clock low and high time should be adjusted to 50% each.^e

Pipeline scheme	"Wavepipelining" with pulsed signal skewed logic ^a in general, partly pass-change logic ^b employed
Vint scheme	2.5V internal voltage • Whether to utilize temperature compensation scheme ^c .
Input pads	• Improve VILL characteristics, that is, undershoot protection. • Put strong enough Vss clamp to CLK, DQM, CS#, DQ pin, at least (Intel's requirement)
CLK buffers	• Small clock buffer to strobe CKE state always except self refresh. • Large clock buffers to strobe all input buffers - control, address, data input, DQM pins. It's been in power-down by CKE. • Both clock buffers use VREF-referenced comparator type for SSTL interface.
CLK buffer for OE	• DLL circuit ^d will be employed to compensate clock-to-output delay for better tAC. • Double clock edges are used at DDR mode. The duty ratio of clock low and high time should be adjusted to 50% each. ^e
CKE Buffer	• Has asynchronous (static) and synchronous buffer. • Async buffer is a part of input delay chain (used for positive set-up time). The output controls asynchronous exit from self refresh. Power-down exit as well (IPDE) ^f ? • Sync. buffer is dynamic latch-typed and its output controls whether large clock, all the other input buffers are enabled. Self refresh command is detected by this as well. • CKE latency is 1 clock cycle for synchronous mode.
All input buffers	• An input buffer consists of input delay chain (power gated by CKE state) and dynamic latch strobed by large clock pulse. • Need to survey better matching delay chain to achieve narrower window of valid input. (Set-up + Hold time) • DDR SDRAM requires +0.5/+0.5ns of setup/hold time of DQ write (Din).
RAS/CAS generator	The same as has been in 16M/64M SDRAM • careful at 2 bank or 4 bank option.

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HR905_148777

4th-Gen. 64M SDRAM Rev.0

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e. Refer to Rambus DRAM. The DLL has duty-ratio adjustment with it.

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Chip Architecture

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Item	Strategy (or issues)
Voltage Generators	• Make best use of well-proven generator circuits since 4M DRAM. • Generate the cookbook design of Vint, VBB, Vpp generators.

- When a pulse is generated, the sizes of inverter chains are emphasized to make only one-side propagation to be much faster than the other. This is simple way to get speed-up, but the pulse width is enlarged through the path.
- Originated by Bob Proebising. It's useful to achieve fast, constant-width, and recovery-free pulse scheme. But it should add some area penalty and complexity in layout. Need to design around due to National Semiconductor's patent issue.
- As temperature goes up, Vint gets a little bit higher. This compensates the speed delay at higher temperature. The production people may not like this idea, because they have seen some problem with Vint at cold temp. The idea to employ temperature detector would be better to trigger this compensation only over some temperature range.
- Actually DLL has been devised to achieve shorter locking time. NEC published its "synchronous mirror delay (SMD)" in 256M SDRAM design. The locking time of SMD is only 2 clock cycles. If this SDRAM will be mounted on the module PCB with PLL component (buffered), then the locking time would be not a concern any more.
- Refer to Rambus DRAM. The DLL has duty-ratio adjustment with it.
- Refer to Samsung's SDRAM spec.
- Used in 2nd-gen 64M SDRAM. It divides the temperature range into 3-4 segments, then different refresh interval is provided. As temperature goes up, data retention time gets worse, so that more frequent refresh should be issued.
- "Short-Side Middle", where global column decoders are.
- Double-ended (MWL & MWL#) in 2nd 64M designs. It caused the stand-by problem when metal bridge let those lines be shorted. Also, lack of 1-decoder redundancy could lower the yield.

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HR905_148780

4th-Gen. 64M SDRAM Rev.0

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updated on 12/19/96

Hynix: July 13, 1998



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07/13/98 06:02 PM

To: Farhad Tabrizi/HEAL
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Subject: Rambus Patent

Dear all,

I have a list of Rambus patents.
Total number of patents are 29 (idea; 1993-1996, idea; 1996-1997).
You can access "IBM Patent Server Home Page" at
<http://www.patents.ibm.com/>
and go to "Patent Number Search", then enter the following numbers.

If anybody has more information, please let me know.

And I want to get a list of SLDRAM's patents. Who can help me?

Followings are list of 29 Rambus patents.

1. 5,243,703
2. 5,254,882
3. 5,268,628
4. 5,319,755
5. 5,325,053
6. 5,337,285
7. 5,355,392
8. 5,357,195
9. 5,390,308
10. 5,408,129
11. 5,432,522
12. 5,436,676
13. 5,432,623
14. 5,436,817
15. 5,446,696
16. 5,455,894
17. 5,473,875
18. 5,485,490
19. 5,488,321
20. 5,499,355
21. 5,498,344
22. 5,521,024
23. 5,523,227
24. 5,537,872
25. 5,554,945
26. 5,572,158
27. 5,578,940

28. 5,596,610
29. 5,606,717

Best Regards,
HakJune Oh

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hjh@sr.hel.co.kr
07/13/98 06:02 PM

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Subject: Rambus Patent

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Rambus

JEDEC Council Meeting - 1997

JEDEC Council Meeting 9/29-30/1997

Strategic Task Group Scope:

Review the scope of the JEDEC Council and brainstorm new ideas for JEDEC to add or delete. Our industry is critical of our (JEDEC) ability to deliver semiconductor component standards which are timely and relevant to its needs. One of our most active committees, the memory committee, is continually getting bad press for not delivering timely and effective standards. Further proof of this can be seen by the formation of parallel groups like PCMCIA, SLD RAM, and RAMBUS. The recent result of this is that the work of these competitive groups has been taken and adopted by JEDEC as our standards. Likewise, we are now adapting the outside work of other national standard groups and issuing them as our own.

Should we create methods that allow such parallel efforts without having to go outside of JEDEC?

The high performance demands of future electronics will force rigorous specification and verification. A 500 MHz microprocessor with a 250 MHz memory bus is happening soon. The requirements for operation at 1 Ghz will separate the men from the boys. The industry will need help and JEDEC is positioned to involve all of the key companies (worldwide) with the industry's best resources.

Are we (JEDEC) prepared to organize and offer such help?

Jedec 0004865

Kelley

29-30 Sep 97

Further proof of this can be seen by the formation of parallel groups like PCMCIA, SLD RAM, and RAMBUS. The recent result of this is that the work of these competitive groups has been taken and adopted by JEDEC as our standards.

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